Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) An integrated circuit comprising:

a standard dimension carrier substrate;

~~an information router integrated on the carrier substrate~~ an application specific integrated circuit die integrated on the carrier substrate wherein an information router and a graphics controller are disposed within the application specific integrated circuit die; [[and]]

system memory operative to store system instructions also integrated on the carrier substrate and in electrical communication with the information router via at least one of a plurality of electrical leads directly connected to the carrier substrate, wherein the system instructions may be stored and retrieved from the system memory through the information router; and

wherein the information router is operative to route the system instructions between a processor external to the standard dimension carrier substrate via an external processor bus, the graphics controller via an internal graphics controller bus and the system memory.

2. (Canceled)

3. (Canceled)

4. (Currently amended) The integrated circuit of claim [[3]]1 further comprising:

graphics memory also integrated on the carrier substrate and in electrical communication with the graphics controller via at least one of the plurality of electrical leads associated with the carrier substrate, wherein graphics information may be stored and retrieved from the graphics memory.

5. (Currently amended) The integrated circuit of claim [[2]]1 wherein the application specific integrated circuit die is coupled to at least one of the plurality of electrical leads associated with the carrier substrate using a plurality of wirebonds.

6. (Currently amended) The integrated circuit of claim [[2]]1 wherein the system memory is disposed on a top surface of the carrier substrate and the application specific integrated circuit die is coupled to a bottom surface of the carrier substrate of the packaged chip using a flip chip technology.

7. (Original) The integrated circuit of claim 1 wherein the system memory is disposed within a chip scale package memory having a plurality of contact pins, wherein the contact pins are soldered to the carrier substrate.

8. (Original) The integrated circuit of claim 1 wherein the system memory is a memory die coupled to the carrier substrate using a plurality of wirebonds.

9. (Original) The integrated circuit of claim 1 wherein the information router within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board.

10. (Currently amended) An integrated circuit comprising:

a standard dimension carrier substrate having a plurality of electrical leads disposed between a top surface and a bottom surface of the carrier substrate;

an application specific integrated circuit die coupled to the bottom surface of the carrier substrate via at least one of the plurality of electrical leads directly connected to the standard dimension carrier substrate, wherein the application specific integrated circuit die includes a north bridge and a graphics controller; [[and]]

system memory operative to store system instructions, the system memory integrated on the top surface of the carrier substrate and in electrical communication with the north bridge via at least one of the plurality of electrical leads directly connected within the carrier substrate, wherein the system instructions may be stored and retrieved from the system memory through the north bridge, within the packaged chip; and

wherein the north bridge is operative to route the system instructions between a processor external to the standard dimension carrier substrate via an external processor bus, the graphics controller via an internal graphics controller bus and the system memory.

11. (Canceled)

12. (Currently amended) The integrated circuit of claim [[11]]10 further comprising:

graphics memory also integrated on the carrier substrate and in electrical communication with the graphics processor via at least one of the plurality of electrical leads within the carrier substrate, wherein graphics information may be stored and retrieved from the graphics memory, within the packaged chip.

13. (Original) The integrated circuit of claim 10 wherein the application specific integrated circuit die is coupled to the bottom surface of the carrier substrate using a plurality of wirebonds.

14. (Original) The integrated circuit of claim 10 wherein the system memory is disposed within at least one chip scale package memory having a plurality of contact pins, wherein the contact pins are soldered to the carrier substrate.

15. (Original) The integrated circuit of claim 10 wherein the system memory is at least one memory die coupled to the carrier substrate using a plurality of wirebonds.

16. (Original) The integrated circuit of claim 10 wherein the north bridge within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board.

17.—20. (Canceled)

21. (Currently amended) An integrated circuit comprising:

a standard dimension carrier substrate including a plurality of electrical leads;

system memory integrated on the standard dimension carrier substrate via at least one of the plurality of electrical leads directly connected to the standard dimension carrier substrate and operative to store processing instructions; [[and]]

an information router integrated on the standard dimension carrier substrate via at least one of the plurality of electrical leads directly connected to the standard dimension carrier substrate and in electrical communication with the system memory, wherein the processing instructions may be stored and retrieved from the system memory through the information router; and

wherein the information router is operative to route the processing instructions between a host processor external to the standard dimension carrier substrate via an external host processor bus, a co-processor external to the standard dimension carrier substrate via an external co-processor bus and the system memory.

22. (Canceled)

23. (Previously presented) The integrated circuit of claim 21 wherein the standard dimension carrier substrate has dimensions of at least one of: a width of between 31 millimeters and 41 millimeters inclusively and a length of between 31 millimeters and 41 millimeters inclusively.